Amendments to the Claims:

Please cancel claims 1-14 and add new claims 15-36 as follows:

15. (New) A semiconductor apparatus containing a low potential reference circuit region and a high potential reference circuit region between which signals are transmitted, the semiconductor apparatus comprising:

a high withstand voltage separating region, which is arranged between the low and high potential reference circuit regions and separating both potential reference circuit regions;

a relay semiconductor device, formed in the high withstand voltage separating region, for transmitting a signal from one of the low and high potential reference circuit regions to the other of them; and

an insulating partition arranged at least between the relay semiconductor device and one of the low and high potential reference circuit regions that is at the output one of the relay semiconductor device, the insulating partition being filled with insulating material in a trench,

wherein output wiring of the relay semiconductor device is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

16. (New) A semiconductor apparatus according to claim 15 further comprising a substrate region arranged below the low and high potential reference circuit regions, wherein

bottom portion of the insulating partition extends to the substrate region, and

the insulation partition surrounds the relay semiconductor device.

17. (New) A semiconductor apparatus according to claim 15 further comprising a group of insulating partitions arranged between the low and high potential reference circuit regions, the group of insulating partitions dividing space between the low and high potential reference circuit regions into plural regions.

18. (New) A semiconductor apparatus according to claim 16 further comprising a group of insulating partitions arranged between the low and high potential reference circuit regions, the group of insulating partitions dividing space between the low and high potential reference circuit regions into plural regions.

19. (New) A semiconductor apparatus according to claim 15,

wherein the high withstand voltage separating region surrounds one of the low and high potential reference circuit regions,

a plurality of the relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region,

each relay semiconductor device is surrounded with the insulating partition, and

output wiring of each relay semiconductor device is wired to an output one of the low and high potential reference circuit regions bridging over the insulating partition.

20. (New) A semiconductor apparatus according to claim 15 further comprising:

a substrate region arranged below the low and high potential reference circuit regions; and

an insulating layer embedded between the low and high potential reference circuit regions and the substrate region, the insulating layer electrically insulating the low and high potential reference circuit regions from the substrate region,

wherein bottom portions of the insulating partitions extend to the insulating layer and the insulating partitions surround the relay semiconductor devices.

21. (New) A semiconductor apparatus according to claim 19 further comprising:

a substrate region arranged below the low and high potential reference circuit regions; and

an insulating layer embedded between the low and high potential reference circuit regions and the substrate region. the insulating layer electrically insulating the low and high potential reference circuit regions from the substrate region,

wherein bottom portions of the insulating partitions extend to the insulating layer and the insulating partitions surround the relay semiconductor devices.

22. (New) A semiconductor apparatus according to claim 15 comprising:

a substrate region of first conduction type;

wherein the low and high potential reference circuit regions are regions of second conduction type formed over a main surface of the substrate region so that one of the regions surrounds the other in separated relation, and

the high withstand voltage separating region is a region formed in a ring shape between the low and high potential reference circuit regions.

23. (New) A semiconductor apparatus according to claim 15 comprising:

a substrate region of either first or second conduction type; and

an insulating film formed on the substrate region;

wherein the low and high potential reference circuit regions are regions of second conduction type formed on the insulating film so that one of the regions surrounds the other in separated relation, and

the high withstand voltage separating region is a region formed in a ring shape between the low and high potential reference circuit regions.

24. (New) A semiconductor apparatus according to ciaim 22, wherein

bottom portion of the insulating partition extends to the substrate region, and

the insulating partition surrounds periphery of a relay semiconductor device from at least three directions.

25. (New) A semiconductor apparatus according to claim 23, wherein

bottom portion of the insulating partition extends to the insulating film, and

the insulating partition surrounds periphery of a relay semiconductor device from at least three directions.

26. (New) A semiconductor apparatus according to claim 22, wherein the high withstand voltage separating region composes junction isolation type structure in which high withstand voltage is maintained by PN junction.

27. (New) A semiconductor apparatus according to claim 23, wherein the high withstand voltage separating region composes junction isolation type structure in which high withstand voltage is maintained by PN junction.

28. (New) A semiconductor apparatus according to claim 22, wherein the high withstand voltage separating region has insulation isolation type structure in which high withstand voltage is maintained by a plurality of insulating partitions.

29. (New) A semiconductor apparatus according to claim 23, wherein the high withstand voltage separating region has insulation isolation type structure in which high withstand voltage is maintained by a plurality of insulating partitions.

30. (New) A semiconductor apparatus according to claim 28, wherein

regions partitioned by the insulating partitions have capacitor structure in which the insulating partitions works as dielectric film, and

potential elevates gradually from the low potential reference circuit region toward the high potential reference circuit region.

31. (New) A semiconductor apparatus according to claim 29, wherein

regions partitioned by the insulating partitions have capacitor structure in which the insulating partitions works as dielectric film, and

potential elevates gradually from the low potential reference circuit region toward the high potential reference circuit region.

32. (New) A semiconductor apparatus according to claim 15 comprising:

a substrate region of first conduction type;

wherein the low and high potential reference circuit regions are regions of second conduction type formed on a main surface of the substrate region so that one of the regions surrounds the other in separated relation, and

a plurality of relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region.

33. (New) A semiconductor apparatus according to claim 15 comprising:

a substrate region of either first or second conduction type; and

an insulating film formed on the substrate region;

wherein the low and high potential reference circuit regions are regions of second conduction type formed on the insulating film so that one of the regions surrounds the other in separated relation, and

a plurality of relay semiconductor devices are arranged to form a ring shape in the high withstand voltage separating region.

34. (New) A semiconductor apparatus according to claim 32, wherein

bottom portion of the insulating partition extends to the substrate region, and

the insulating partition surrounds periphery of a relay semiconductor device from at least three directions.

35. (New) A semiconductor apparatus according to claim 33, wherein

bottom portion of the insulating partition extends to the insulating film, and

the insulating partition surrounds periphery of a relay semiconductor device from at least three directions.

36. (New) A semiconductor apparatus according to claim 19

comprising a substrate region of first conduction type,

wherein the low and high potential reference circuit regions are regions of second conduction type formed over a main surface of the

substrate region so that one of the regions surrounds the other in separated relation.